IN THE CLAIMS

Please amend the claims as follows:

1. (original) A memory device comprising, in a single integrated circuit package:

a static memory means (10, 12) defining at least first and second nodes (A, B) communicatively connected with read and/or write data lines;

at least one non-volatile memory means (14, 16) associated with said static memory means (10, 12), and writing data stored therein to said static memory means (10, 12); said non-volatile memory means comprising a first non-volatile element (14) having a control gate connected to a first node (B) and a source connected to a second node (A), and a second non-volatile element (16) having a control gate connected to the second node (A) and a source connected to the first node (B), the drain of each non-volatile element (14, 16) being connected by means of a respective transistor (18, 20) to a supply means (VDP); characterized in that said respective transistors are arranged to isolate the drains of the first and second non-volatile elements from the supply means during a program cycle of the memory device.

2. (original) A memory device according to claim 1, wherein said non-volatile memory elements (14, 16) comprise embedded flash or EEPROM elements.

3. (currently amended) A memory device according to claim 1~~ or 2~~, wherein said non-volatile memory elements (14, 16) comprise double or single poly floating gate type memory cells.

4. (original) A memory device according to claim 1, wherein said non-volatile memory elements (14, 16) comprise devices which can be programmed and erased by means of tunneling of charges.

5. (currently amended) A memory device according to ~~any one of claims 1 to 4~~claim 1, wherein the non-volatile memory elements (14, 16) are programmed with opposite data.

6. (currently amended) A memory device according to ~~any one of claims 1 to 5~~claim 1, wherein the static memory means comprises a pair of cross-coupled inverters (10, 12).

7. (currently amended) A memory device according to ~~any one of claims 1 to 6~~claim 1, wherein one or more respective selection

transistors (22) are provided, by means of which the nodes (A, B) are communicatively coupled to the read and/or write lines.

8. (currently amended) A memory device according to ~~any one of claims 1 to 7~~claim 1, including one or more isolation transistors (24).

9. (currently amended) A reconfigurable programmable logic device including a memory device according to ~~any one of claims 1 to 8~~claim 1.

10. (currently amended) A field programmable gate array including a memory device according to ~~any one of claims 1 to 9~~claim 1.